REMARKS

Claims 1-13 stand cancelled, and claim 24 has been cancelled. New claims 25-27 have been added. No new matter is presented by virtue of the within amendments. Support therefore can be found throughout the application. For instance, support for new claims 25-27 appears at least at page 3, lines 1-11, page 7, lines 26-30, page 9, lines 5-9, and page 11, lines 19-26 of the specification as originally filed.

Claims 19 and 20 stand rejected under 35 U.S.C. §112, second paragraph. The Office Action goes on to state terms appearing in the noted claims which allegedly render the subject matter thereof indefinite or otherwise misdescriptive.

The rejection of claim 19 is traversed. Applicants wish to clarify to the Examiner the claim 19 recitation of the voltage on the circuit node below the at least one threshold value. This value does not suggest that the voltage on the circuit node is below some other voltage by the threshold value. Rather, the voltage is below the threshold value itself. Applicants respectfully request withdrawal of the rejection.

The rejection of claim 20 also is traversed and the following clarification is offered. Applicants acknowledge that when the signal ENQ is low, transistor P5 is conducting. However, transistor P6 is switched to a non-conducting state. Therefore, even if transistor P5 is conducting, it cannot conduct current anywhere since its load section is connected to voltage U_{10}, transistor P6, and the gate of transistor N2, so that no current may flow.

In view of the within explanation/clarification provided above, reconsideration and withdrawal of the §112, 2nd paragraph rejections are requested.

Claims 14-24 stand rejected under 35 U.S.C. §102(b) over Ajit et al. (Publication No. US 2003/0122606A1).

The rejection is traversed. The cited reference does not teach or suggest the driver circuit of the present invention in any manner sufficient to sustain the §102

rejection. Indeed, several features of the present invention are not taught or suggested by Ajit et al.

For instance, Ajit et al. does not disclose the instant claim 14 recitation of an electrical path from the circuit node to the reference potential, which electrical path has at least one diode to pre-set the at least one threshold value. Those of ordinary skill in the art will recognize that an electrical path is a path over which conduction may occur, at least when the path is activated. Activation can take place by a switch. The electrical path of the instant invention is demonstrated at least in figure 1, and comprises diodes D2-D4, transistor (switch) P4, and resistor R1. Claim 14 of the instant invention therefore provides a path comprising only elements which may conduct current over the path, provided that transistor P4 is activated by the ENQ signal and the threshold voltages of diodes D2-D4 are exceeded.

Ajit et al. does not teach or suggest such a path. Indeed, attention is directed to figure 18 of Ajit et al. which shows diode 905; however, the electrical path between the circuit node 309 and reference potential does not include diode 905. Additionally, as shown in figure 11D of Ajit et al., device 901 does not include the electrical path recited in the instant claim 14, as the input generally ends at the gates of the transistors. Thus, the claim 14 feature of an electrical path that has at least one diode to pre-set the at least one threshold value is not taught or suggested by Ajit.

Additionally, Ajit et al. does not disclose the present claim 19 recitation of an electrical path, which comprises the load section of a transistor controlled by the enabling signal, said transistor being connected on the one hand with a further voltage and on the other hand with a diode and serves to regulate the control voltages in the inactive state, as long as the voltage on the circuit node is below the at least one threshold value. Again, figure 1 of the present invention demonstrates, for transistors P2 and N2, an electrical path from potential U_{core} via P3 and D1 to the gate of transistor P2 further via P6 to the gate of transistor N2.

The Office Action asserts that figure 18 of Ajit et al. elements 901, 905, 907, and

909b form an electrical path. However, it is noted that elements 907 and 909b form separate branches, i.e. separate paths. Additionally as shown in figure 11D of Ajit et al., device 901 does not include the electrical path recited in the instant claim 19, as the input generally ends at the gates of the transistors. Thus, the electrical path feature recited in claim 19 is not taught or suggested by Ajit et al.

Further, regarding present claim 20, it is respectfully submitted that Ajit et al. does not disclose the claim 20 recitation of a driver circuit that is configured in such a manner that in the active state it consumes no static power.

The Office Action takes the position that figure 11D of Ajit et al. shows that when the signal OE is in an enabling state, the PMOS transistors of figure 11D are turned off and no current flows from voltage V_{DDP} to voltage V_{DDC}, thus no static power is consumed. However, circuit 901 comprises a plurality of paths between V_{DDP} to V_{DDC}, only one of which comprises a PMOS transistor, which is coupled to the signal OE. Others transistors are influenced by the voltage on the pad. It follows then that depending on the voltage on the pad, at least one of the pads in figure 11D becomes conductive, and as a result, the circuit consumes static power. Thus, the feature of claim 20 that the driver circuit be configured in such a manner that in the active state, consumes no static power, is not taught or suggested by Ajit et al.

Lastly, it is noted that the circuit arrangement disclosed by Ajit et al. requires two first bias circuits for biasing each of the transistors 301-307 separately. In contrast thereto, in the non-active state of the present invention, transistor P6 is conductive and therefore the gates of transistors P2 and N2 are connected, making it possible to control both transistors with the same driver circuit. This feature is clearly distinct from Ajit et al. and is embodied in new claims 25-27 of the present application.

Accordingly, the §102 rejection is properly withdrawn. For example, see *In re Marshall*, 198 USPQ 344, 346 (CCPA 1978) ("[r]ejections under 35 U.S.C. §102 are proper only when the claimed subject matter is identically disclosed or described in the prior art.")

In view thereof, reconsideration and withdrawal of the §102 rejection are thus requested.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Dated: June 1, 2005

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